

Features

- Input Voltage Range: 2.4 V to 5.5 V
- Output Voltage Options:
 - ◆ Fixed Voltage: 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 2.9 V, 3 V, 3.3 V
 - ◆ Adjustable Voltage: 0.8 V to 5 V
- High Output Accuracy:
 - ◆ $\pm 1\%$ Typical Under Room Temperature
 - ◆ $\pm 2\%$ Through Operating Conditions
- Maximum Output Current: 500 mA
- Low Dropout Voltage: 400 mV at 500 mA
- Low Quiescent Current and Shutdown Current
- Foldback Current Limit and Thermal Protection
- Stable with 2.2 μF Ceramic Capacitor
- Inrush Input Current Limitation During Start-up
- Thermal Shutdown Protection
- Operating Temperature Range: -40°C to $+85^{\circ}\text{C}$
- Junction Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Package: SOT23-5, SC70-5, SOT89-3, 1 \times 1 DFN-4

Applications

- Handheld Devices with Battery Power Supply
- POS
- Video Surveillance
- Wireless and IoT modules

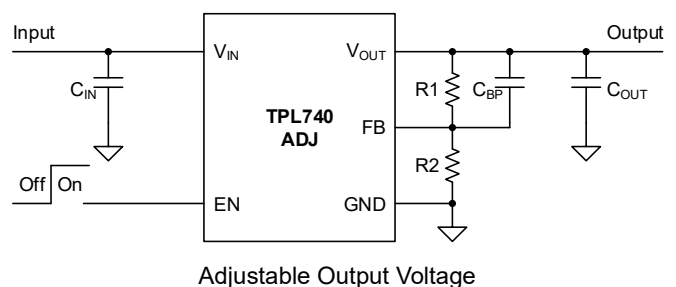
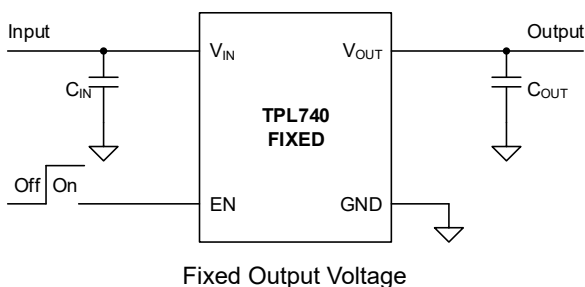
Description

The TPL740 series products are high performance and low dropout linear regulators. The TPL740 series products support maximum 500 mA output current with low quiescent current and high PSRR. The TPL740 series products is stable with ceramic output capacitor from 2.2 μF to 10 μF .

The TPL740 series products have a high PSRR with 60 dB at 1 KHz. This feature makes TPL740 series products very suitable for power-sensitive applications with high noise from previous stage power supply. As low as 49 μA quiescent current and only 20 nA shutdown current makes the TPL740 series products ideal choices for portable devices with battery power supply. Current-limit foldback and thermal overload protection circuits improves the reliability under heavy load conditions.

The TPL740 series products provide several output voltage version options including fixed version and adjustable version with $\pm 2\%$ output voltage accuracy over operating conditions. The TPL740 series products are guaranteed over operating temperature range from -40°C to $+85^{\circ}\text{C}$.

Typical Application Schematic



Product Family Table

Part Number	Output Voltage	Order Number	Package	Transport Media, Quantity	MSL	Marking Information
TPL740ADJ	Adjustable (0.8 V ~ 5 V)	TPL740ADJ-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2A
TPL740F12	Fixed 1.2 V	TPL740F12-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2D
TPL740F15	Fixed 1.5 V	TPL740F15-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2K
TPL740F18	Fixed 1.8 V	TPL740F18-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2F
TPL740F25	Fixed 2.5 V	TPL740F25-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2G
TPL740F27	Fixed 2.7 V	TPL740F27-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2L
TPL740F28	Fixed 2.8 V	TPL740F28-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2H
TPL740F29	Fixed 2.9 V	TPL740F29-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2M
TPL740F30	Fixed 3.0 V	TPL740F30-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2I
TPL740F33	Fixed 3.3 V	TPL740F33-5TR	SOT23-5	Tape and Reel, 3,000	L3	L2J
TPL740ADJ	Adjustable (0.8 V ~ 5 V)	TPL740ADJ-CR	SC70-5	Tape and Reel, 3,000	L3	L2A
TPL740F12	Fixed 1.2 V	TPL740F12-CR	SC70-5	Tape and Reel, 3,000	L3	L2D
TPL740F15	Fixed 1.5 V	TPL740F15-CR	SC70-5	Tape and Reel, 3,000	L3	L2K
TPL740F18	Fixed 1.8 V	TPL740F18-CR	SC70-5	Tape and Reel, 3,000	L3	L2F
TPL740F25	Fixed 2.5 V	TPL740F25-CR	SC70-5	Tape and Reel, 3,000	L3	L2G
TPL740F27	Fixed 2.7 V	TPL740F27-CR	SC70-5	Tape and Reel, 3,000	L3	L2L
TPL740F28	Fixed 2.8 V	TPL740F28-CR	SC70-5	Tape and Reel, 3,000	L3	L2H
TPL740F29	Fixed 2.9 V	TPL740F29-CR	SC70-5	Tape and Reel, 3,000	L3	L2M
TPL740F30	Fixed 3.0 V	TPL740F30-CR	SC70-5	Tape and Reel, 3,000	L3	L2I
TPL740F33	Fixed 3.3 V	TPL740F33-CR	SC70-5	Tape and Reel, 3,000	L3	L2J
TPL740F12	Fixed 1.2 V	TPL740F12-89TR	SOT89-3	Tape and Reel, 4,000	L3	L2D
TPL740F15	Fixed 1.5 V	TPL740F15-89TR	SOT89-3	Tape and Reel, 4,000	L3	L2K
TPL740F18	Fixed 1.8 V	TPL740F18-89TR	SOT89-3	Tape and Reel, 4,000	L3	L2F
TPL740F25	Fixed 2.5 V	TPL740F25-89TR	SOT89-3	Tape and Reel, 4,000	L3	L2G
TPL740F27	Fixed 2.7 V	TPL740F27-89TR	SOT89-3	Tape and Reel, 4,000	L3	L2L
TPL740F28	Fixed 2.8 V	TPL740F28-89TR	SOT89-3	Tape and Reel, 4,000	L3	L2H
TPL740F29	Fixed 2.9 V	TPL740F29-89TR	SOT89-3	Tape and Reel, 4,000	L3	L2M
TPL740F30	Fixed 3.0 V	TPL740F30-89TR	SOT89-3	Tape and Reel, 4,000	L3	L2I
TPL740F33	Fixed 3.3 V	TPL740F33-89TR	SOT89-3	Tape and Reel, 4,000	L3	L2J

Product Family Table (continued)

Part Number	Output Voltage	Order Number	Package	Transport Media, Quantity	MSL	Marking Information
TPL740F12	Fixed 1.2 V	TPL740F12-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L2D
TPL740F15	Fixed 1.5 V	TPL740F15-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L2K
TPL740F18	Fixed 1.8 V	TPL740F18-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L2F
TPL740F25	Fixed 2.5 V	TPL740F25-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L2G
TPL740F27	Fixed 2.7 V	TPL740F27-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L2L
TPL740F28	Fixed 2.8 V	TPL740F28-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L2H
TPL740F29	Fixed 2.9 V	TPL740F29-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L2M
TPL740F30	Fixed 3.0 V	TPL740F30-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L2I
TPL740F33	Fixed 3.3 V	TPL740F33-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L2J

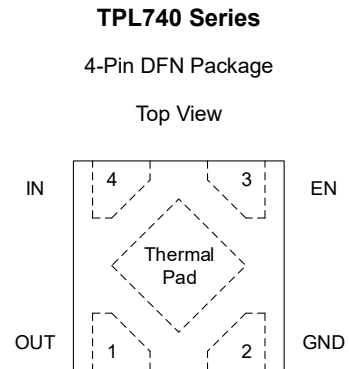
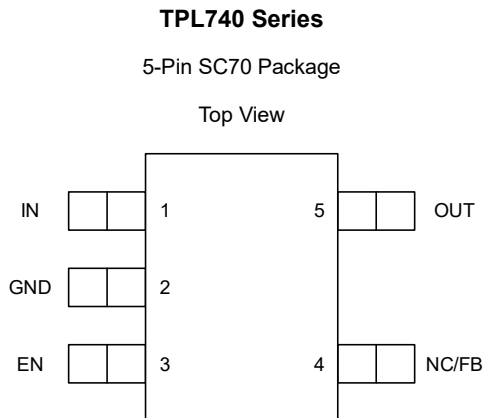
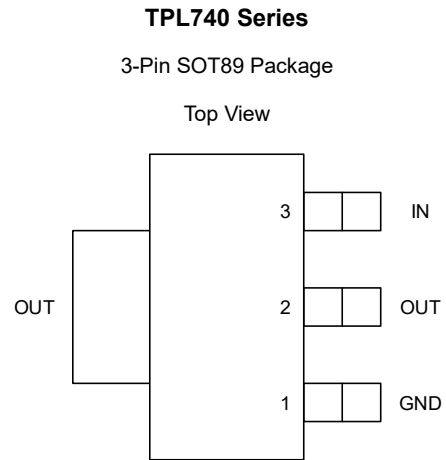
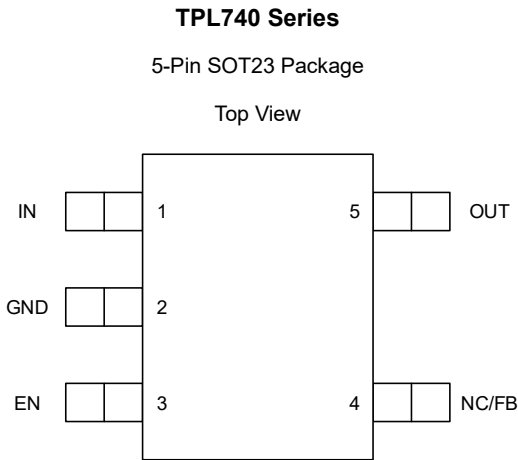
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Revision History

Date	Revision	Notes
2018/8/28	Rev.Pre	Preliminary Version
2018/11/26	Rev.A.0	Initial Release
2019/02/11	Rev.A.1	<ol style="list-style-type: none">Added 1.5 V, 2.7 V, 2.9 V voltage optionsAdded Link of Figure 11 and Figure 12
2019/08/08	Rev.A.2	<ol style="list-style-type: none">Added max limit of item: I_{GND}, I_{SHDN}, UVLO, Load regulation, V_{DO}
2020/08/15	Rev.A.3	<ol style="list-style-type: none">Change “Soft-start Limits Input Current Surge During Enable” to “Inrush Input Current Limitation During Start-up”Add description of “Short-Circuit Protection”

Pin Configuration and Functions



Pin Functions

Name	Pin Number				I/O	Description
	SOT23-5	SC70-5	SOT89-3	DFN-4		
IN	1	1	3	4	I	Input voltage pin. Bypass IN to GND with a 1 μ F or greater capacitor.
OUT	5	5	2	1	O	Regulated output voltage pin. Bypass OUT to GND with a 2.2 μ F or greater capacitor.
EN	3	3	-	3	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
GND	2	2	1	2	-	Ground reference pin. Connect GND pin to PCB ground plane directly.
NC	4	4	-	-	-	No connection.
FB	4	4	-	-	I	Output feedback pin (Adjustable version only). Connect to a resistor divider to adjust the output voltage.

Note: Thermal pad must be connected to PCB ground plane to maximum the thermal performance.

Specifications

Absolute Maximum Ratings

Parameters		Min	Max	Unit
V_{IN}, V_{EN}	Input Voltage	-0.3	6	V
V_{OUT}	Output Voltage	-0.3	6	V
V_{FB}	Feedback Voltage (Adjustable version only)	-0.3	6	V
T_J	Junction Temperature Range	-40	150	°C
T_{STG}	Storage Temperature Range	-65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±2	kV

Recommended Operating Conditions

Parameters		Min	Max	Unit
V_{IN}	Input Voltage	2.4	5.5	V
V_{EN}	Enable Voltage	0	V_{IN}	V
V_{OUT}	Output Voltage	0	5	V
V_{FB}	Feedback Voltage (Adjustable version only)	0	V_{OUT}	V
I_{OUT}	Output Current	0	500	mA
T_J	Junction Temperature Range	-40	125	°C
T_A	Operating Temperature Range	-40	85	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	280	62	°C/W
SC70-5	310	80	°C/W
SOT89-3	55	88	°C/W
1×1 DFN-4	210	110	°C/W

Electrical Characteristics

All test condition: $V_{IN} = V_{OUT(NOM)} + 0.5V$ or $2.4 V$, whichever is greater; $C_{OUT} = 2.2 \mu F$, $T_A = +25^\circ C$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input voltage range		2.4		5.5	V
I_{GND}	Ground pin current	$I_{OUT} = 0 \text{ mA}$		49	200	μA
		$I_{OUT} = 100 \text{ mA}$		200	2000	μA
I_{SHDN}	Shutdown current	EN = GND		0.02	2	μA
UVLO	V_{IN} under-voltage-lock-out	V_{IN} rising	1.5	1.9	2.4	V
		Hysteresis		200		mV
Enable Input Voltage and Current						
$V_{IH(EN)}$	EN logic-input high level (enable)		1.2		V_{IN}	V
$V_{IL(EN)}$	EN logic-input low level (disable)		0		0.4	V
I_{EN}	EN pin leakage current	EN = 5V		1	3	μA
Regulated Output Voltage and Current						
V_{OUT}	Output voltage accuracy	$T_J = +25^\circ C$		1%		
		$-40^\circ C \leq T_J \leq +125^\circ C$	-2%		2%	
V_{FB}	Feedback pin voltage	ADJ version only	0.784	0.8	0.816	V
ΔV_{OUT}	Line regulation	$V_{IN} = 2.4V$ or $V_{OUT(NOM)} + 0.5 V$ to $5.5 V$, or $V_{IN} \geq 2.4V$, $I_{OUT} = 1 \text{ mA}$		1	5	mV
	Load regulation	$I_{OUT} = 1 \text{ mA}$ to 500 mA		20	60	mV
$V_{DO}^{(1)}$	Dropout voltage	$V_{IN} = 0.98 \times V_{OUT(NOM)}$, $I_{OUT} = 100 \text{ mA}$		75	100	mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$, $I_{OUT} = 300 \text{ mA}$		200	250	mV
		$V_{IN} = 0.98 \times V_{OUT(NOM)}$, $I_{OUT} = 500 \text{ mA}$		300	400	mV
I_{OUT}	Output current	V_{OUT} in regulation	0		500	mA
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	550	1000	1400	mA
PSRR	Power supply rejection ratio (fixed version)	$I_{OUT} = 100 \text{ mA}$, $f = 1 \text{ kHz}$		60		dB
		$I_{OUT} = 100 \text{ mA}$, $f = 100 \text{ kHz}$		40		dB
		$I_{OUT} = 100 \text{ mA}$, $f = 1 \text{ MHz}$		40		dB
	Power supply rejection ratio (ADJ version)	$I_{OUT} = 100 \text{ mA}$, $f = 1 \text{ kHz}$, $C_{BP} = 100 \text{ nF}$		65		dB
		$I_{OUT} = 100 \text{ mA}$, $f = 100 \text{ kHz}$, $C_{BP} = 100 \text{ nF}$		60		dB
		$I_{OUT} = 100 \text{ mA}$, $f = 1 \text{ MHz}$, $C_{BP} = 100 \text{ nF}$		45		dB
V_N	Output noise voltage (fixed version)	$I_{OUT} = 100 \text{ mA}$, BW = 100Hz to 80 kHz		130		μV_{RMS}
	Output noise voltage (ADJ version)	$I_{OUT} = 100 \text{ mA}$, BW = 100Hz to 80 kHz, $C_{BP} = 100 \text{ nF}$		40		μV_{RMS}

(1) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: $V_{IN} - V_{DROPOUT}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Regulated Output Voltage and Current						
$t_{STR}^{(2)}$	Start-up time (fixed version)	$I_{OUT} = 500 \text{ mA}$, $C_{OUT} = 2.2 \mu\text{F}$		150		μs
	Start-up time (ADJ version)	$I_{OUT} = 500 \text{ mA}$, $C_{OUT} = 2.2 \mu\text{F}$, $C_{BP} = 100 \text{ nF}$		15		ms
Temperature Range						
T_{SD}	Thermal shutdown temperature			170		$^{\circ}\text{C}$
	Thermal shutdown hysteresis			30		$^{\circ}\text{C}$

(2) Start-up time from EN assertion to $0.98 \times V_{OUT(NOM)}$.

Typical Performance Characteristics

All test condition: $V_{IN} = V_{OUT(NOM)} + 0.5V$ or $2.4V$, whichever is greater; $C_{OUT} = 2.2 \mu F$, $T_A = +25^\circ C$, unless otherwise noted.

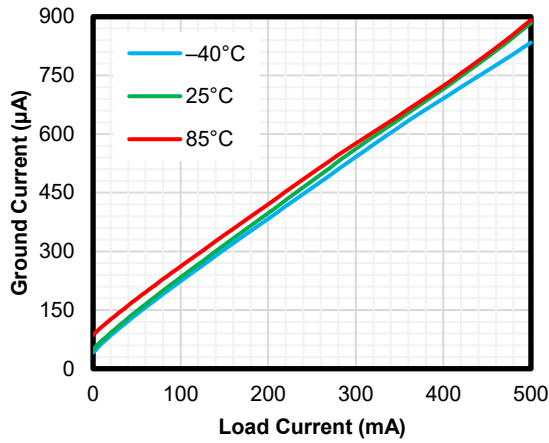


Figure 1 Quiescent Current vs Output Current

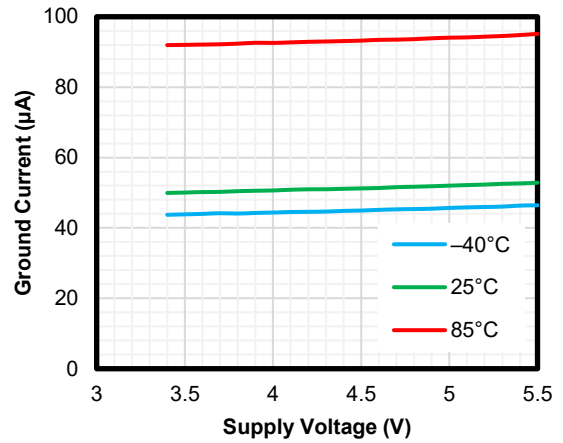


Figure 2 Quiescent Current vs Input Voltage

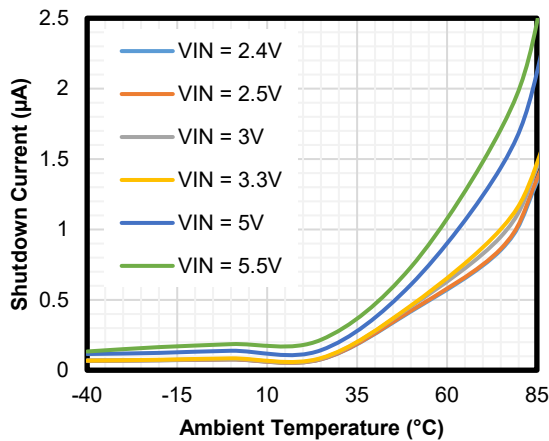


Figure 3 Shutdown Current vs Ambient Temperature

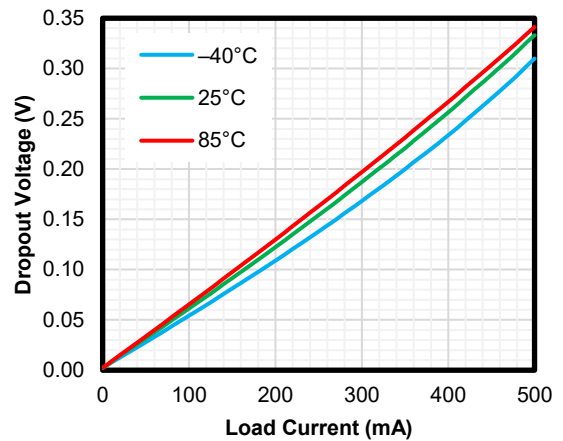


Figure 4 Dropout Voltage vs Output Current

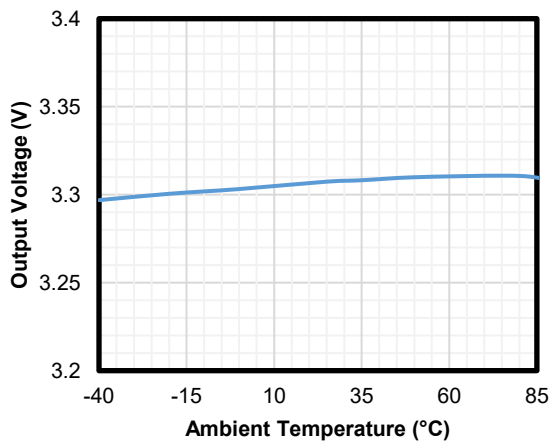


Figure 5 Output Accuracy vs Ambient Temperature

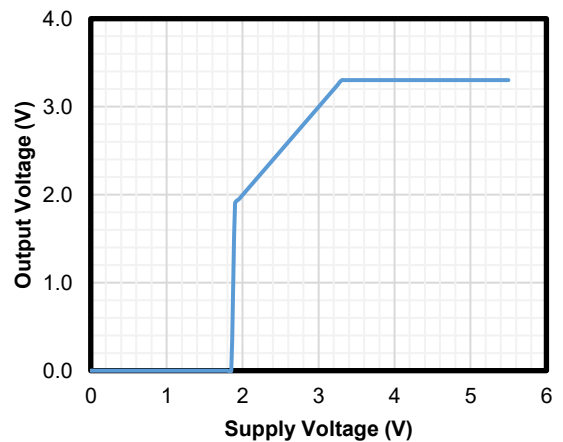


Figure 6 Output Voltage vs Input Voltage

Typical Performance Characteristics (continued)

Test condition: $V_{IN} = V_{OUT(NOM)} + 0.5V$ or $2.4 V$, whichever is greater; $C_{OUT} = 2.2 \mu F$, $T_A = +25^\circ C$, unless otherwise noted.

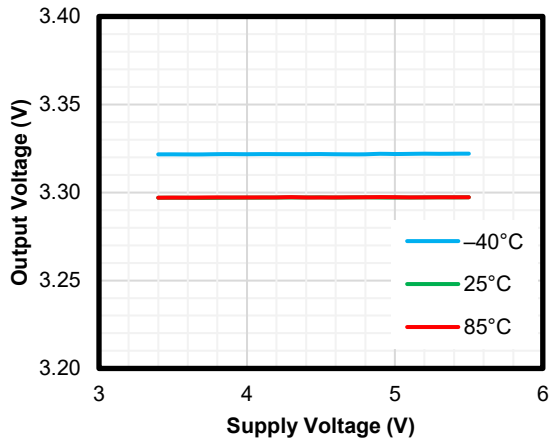


Figure 7. Line Regulation

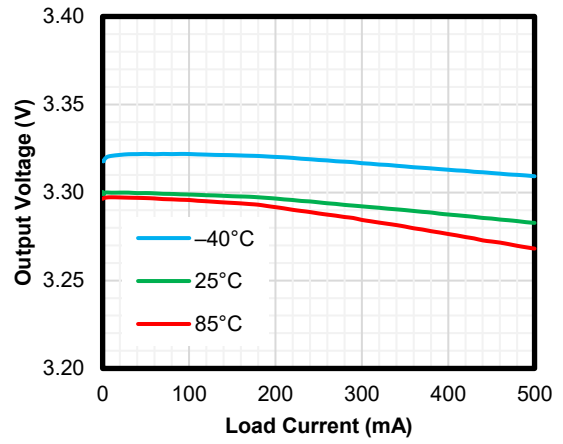


Figure 8. Load Regulation

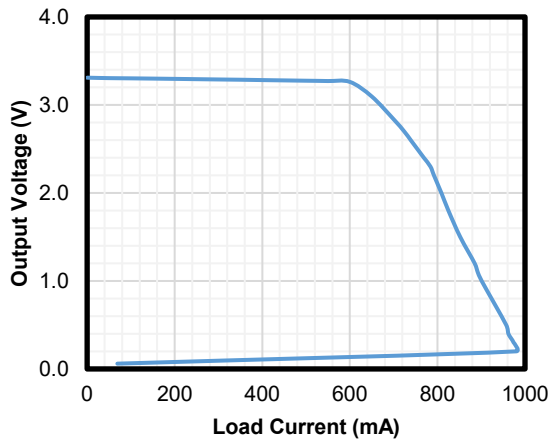


Figure 9. Foldback Current Limit

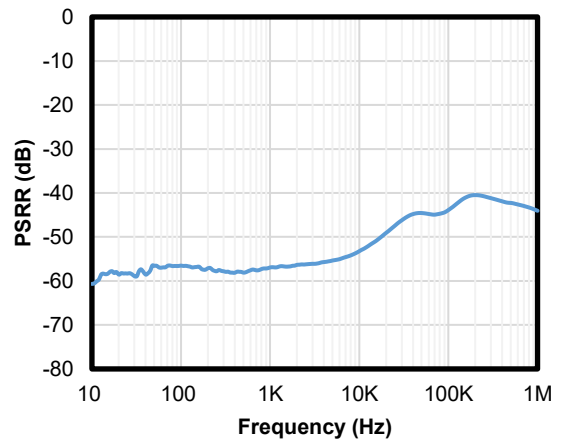


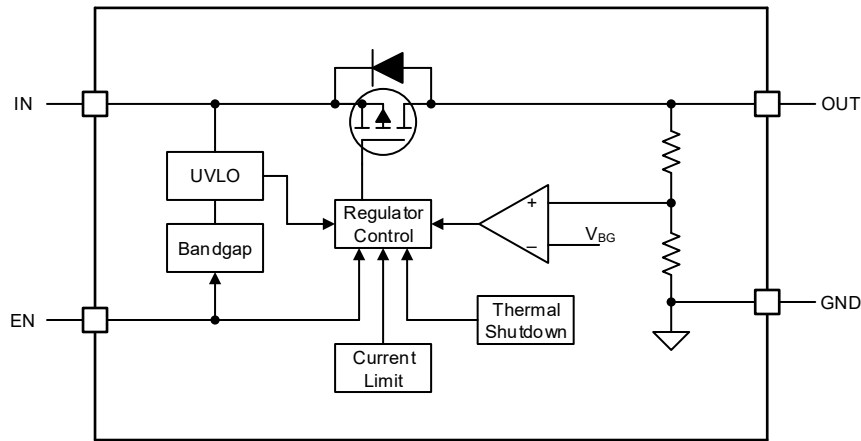
Figure 10. PSRR

Detailed Description

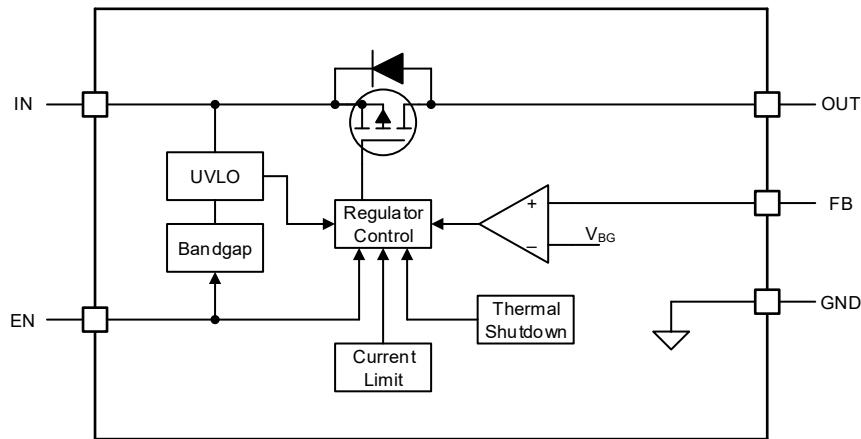
Overview

The TPL740 devices products are 500 mA high PSRR, low-dropout linear regulators with very low quiescent current. These voltage regulators operate from 2.4 V to 5.5 V and consume 49 μ A of quiescent current at no load and only 20 nA when in shutdown mode. The TPL740 series are available in fixed voltage versions of 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 2.9 V, 3 V and 3.3 V, and also adjustable voltage version of 0.8 V to 5 V with $\pm 2\%$ output voltage accuracy over operating conditions.

Functional Block Diagram



TPL740 Series Fixed Output Version



TPL740 Series Adjustable Output Version

Feature Description

Enable

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Under-voltage Lockout (UVLO)

The TPL740 series use an under-voltage lockout circuit (UVLO = 1.9 V) to keep the output shut off until the internal circuitry operates properly.

Regulated Output Voltage

The TPL740 series are available in fixed voltage versions of 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 2.9 V, 3 V and 3.3 V. When the input voltage is higher than $V_{OUT(NOM)} + V_{DO}$ or 2.4V, output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT(NOM)} + V_{DO}$ or 2.4V, output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below UVLO threshold, the output keeps shut off.

Adjustable Output Voltage

The TPL740 series are also available in adjustable voltage versions of 0.8 V to 5 V by selecting suitable external resistor dividers. Use [Equation 1](#) to calculate the output voltage ($V_{FB} = 0.8$ V). Suggest select resistor value of (R1 + R2) between 10 k Ω and 100 k Ω .

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2} \right) \quad (1)$$

Current Limit

The TPL740 series integrate an internal foldback current limit that helps to protect the regulator during fault conditions. When the output is shorted, the LDO supplies a typical current of 100 mA. Output voltage is not regulated when the device is in current limit and is $V_{OUT} = I_{CL} \times R_{LOAD}$.

Short-Circuit Protection

The TPL740 series integrate a short-circuit protection. When the output pin is shorted to ground or forced to a voltage below 0.2V, the output current of the TPL740 series is limited to a typical value of 150 mA.

Thermal Shutdown

During normal operation, LDO junction temperature should not exceed 125°C. When the junction temperature exceeds the thermal shutdown threshold, the LDO shut down the output immediately. Until when the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the output turns on again.

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL740 devices are a series of 500 mA high PSRR, low-dropout linear regulator with low quiescent current. The following application schematic shows a typical usage of the TPL740 series.

Typical Application

Figure 11 and Figure 12 show the typical application schematic of the TPL740 series.

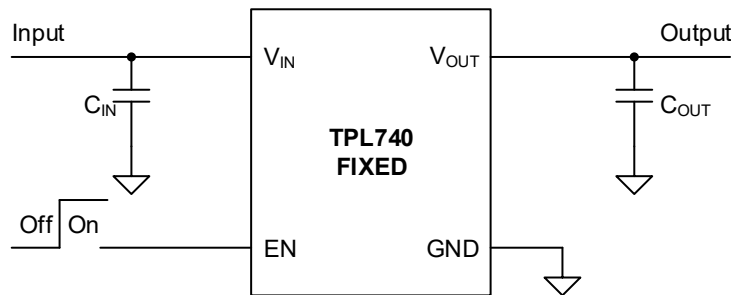


Figure 11 TPL740 Fixed Output Voltage

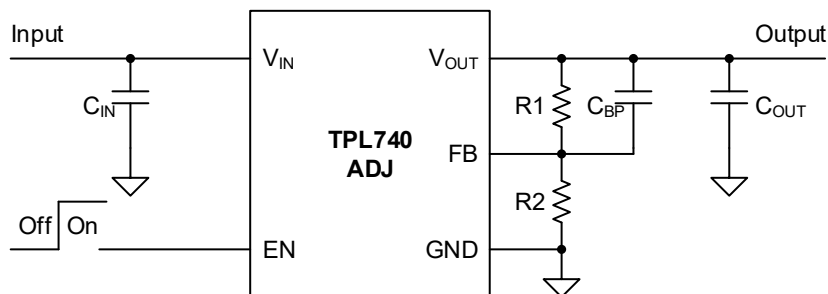


Figure 12 TPL740 Adjustable Output Voltage

Input Capacitor and Output Capacitor

3PEAK recommends adding a 1 μF or greater capacitor with a 0.1 μF bypass capacitor in parallel at IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL740 series requires an output capacitor with a minimum effective capacitance value of 2.2 μF . 3PEAK recommends selecting a X5R- or X7R-type ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using [Equation 2](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (2)$$

The junction temperature can be estimated using [Equation 3](#). θ_{JA} is the junction-to-ambient thermal resistance (See Section [Thermal Information](#)).

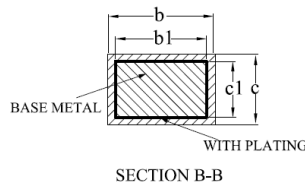
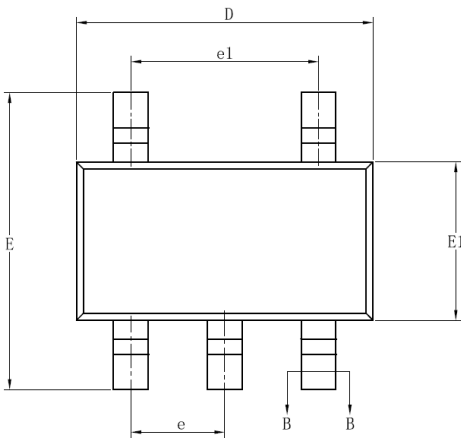
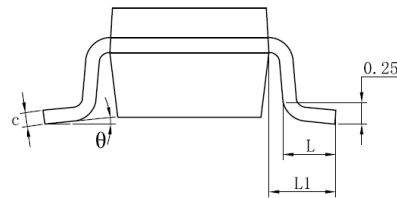
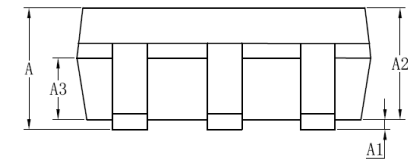
$$T_J = T_A + P_D \times \theta_{JA} \quad (3)$$

Layout Requirements

- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the input pin to ground with a 0.1 μ F bypass capacitor. The loop area formed by the bypass capacitor connection, IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.

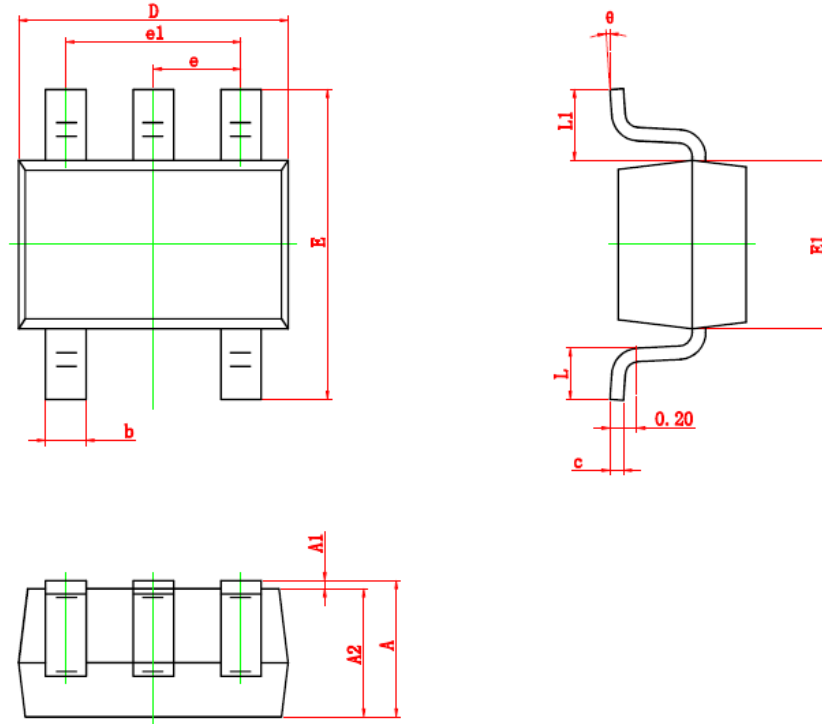
Package Outline Dimensions

SOT23-5



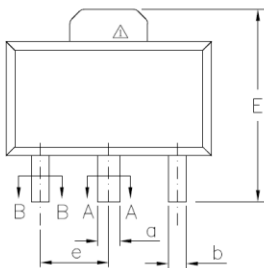
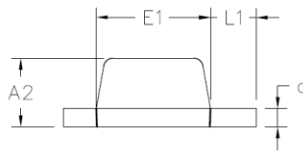
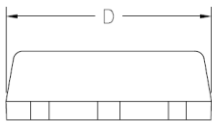
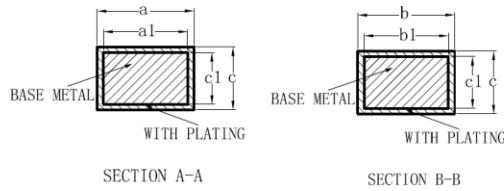
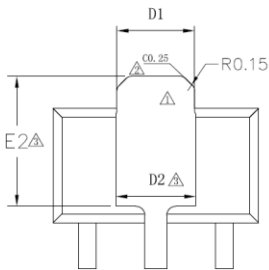
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.25
A1	0.04	—	0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
e1	1.90BSC		
L	0.30	—	0.60
L1	0.60REF		
θ	0	—	8°

SC70-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.260	0.460	0.010	0.018
L1	0.525 REF.		0.021 REF.	
θ	0°	8°	0°	8°

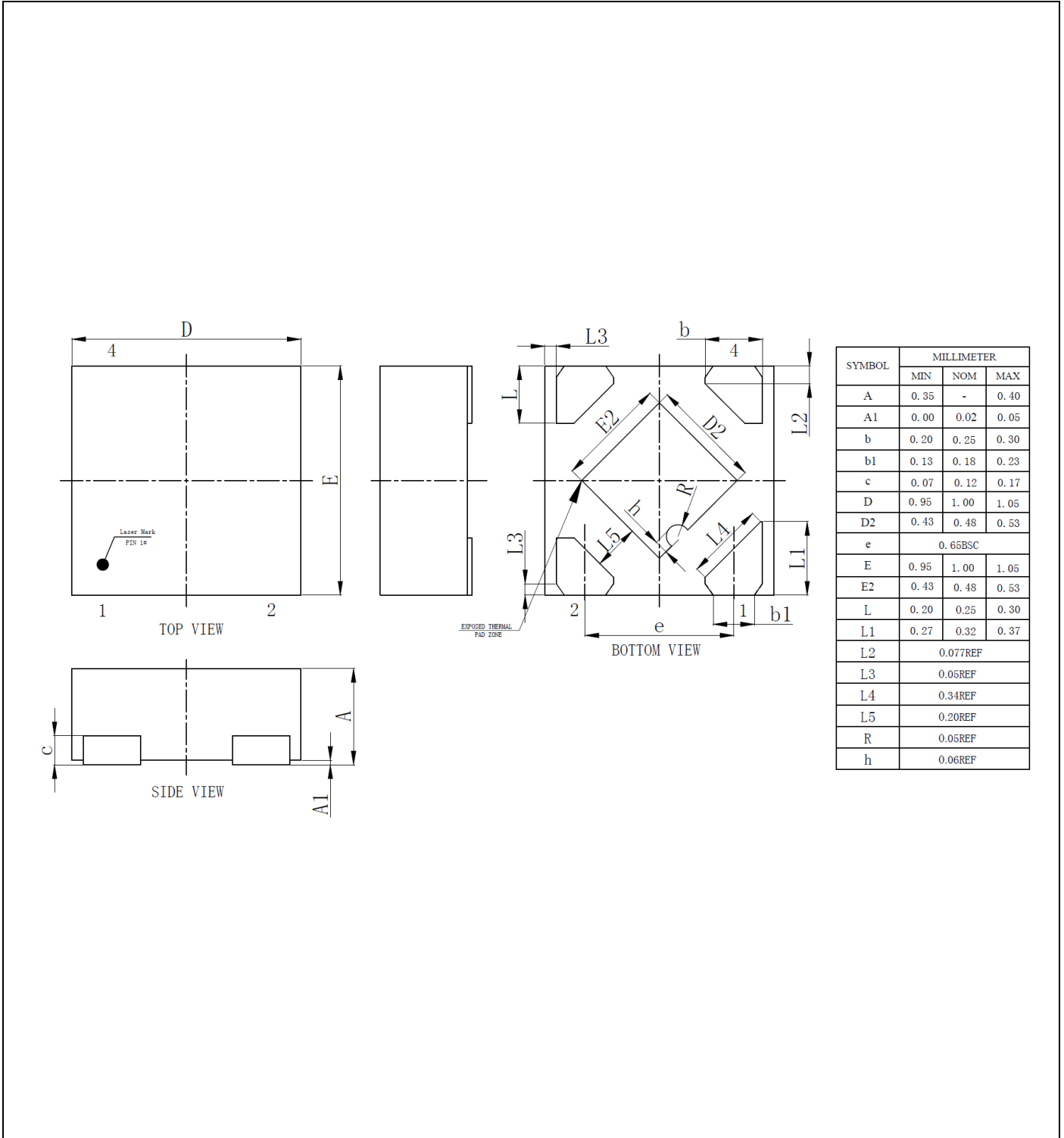
SOT89-3



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A2	1.40	1.50	1.60
b	0.38	—	0.46
b1	0.37	0.40	0.43
c	0.38	—	0.42
c1	0.37	0.38	0.39
a	0.46	—	0.56
a1	0.45	0.48	0.51
D	4.40	4.50	4.60
D1	1.62	—	1.83
E	3.95	—	4.25
E1	2.40	2.50	2.60
e	1.50BSC		
L1	0.89	—	1.20

Size (mm)	D2	E2
L/F Size (mm)		
66.9*63	1.75REF	2.84REF

1×1 DFN-4



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