DIO6913
High-Efficiency 3A, 24V Input Synchronous Step Down Converter

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom) 80mΩ/40mΩ, 3.0A
- 4.5-24V input voltage range
- High-Efficiency Synchronous-Mode
- Internal soft start limits the inrush current
- Over Current protection
- Thermal shutdown
- Available in TSOT23-6 package

Descriptions

The DIO6913 is high-efficiency, high frequency synchronous step-down DC-DC regulator ICs capable of delivering up to 3A output currents. The DIO6913 family operate over a wide input voltage range from 4.5V to 24V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

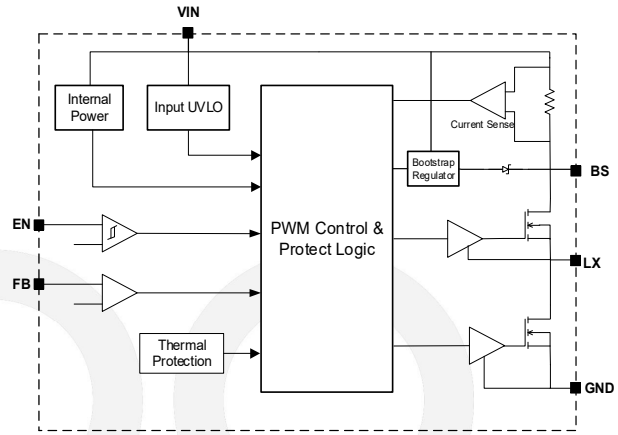
The COT architecture with Pseudo fixed switching frequency operation provides fast transient response and eases loop stabilization. Protection features include over-current protection and thermal shutdown.

The DIO6913 requires a minimal number of readily-available, standard, external components and is available in a space-saving TSOT23-6 package.

Applications

- Portable Navigation Device
- Set Top Box
- Portable TV
- LCD TV

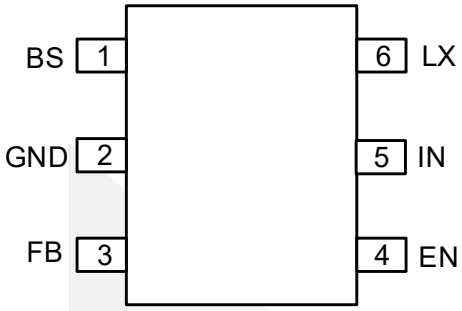
Function Block



Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO6913TST6	13YW	Green	-40 to 85°C	TSOT23-6	Tape & Reel, 3000

Pin Assignments



TSOT23-6

Figure 1 Pin Assignment (Top View)

Pin Definitions

Pin Name	Description
BS	Bootstrap. Connect a capacitor and a resistor between LX and BS pins to form a floating supply across the high-side switch driver. Recommend to use 0.1μF BS capacitor.
GND	Power Ground
FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.6*(1+R1/R2).Add optional C2 (10pF~47pF) to speed up the transient response.
EN	Enable control. Pull high to turn on. Do not float.
IN	Power Input
LX	Inductor pin. Connect this pin to the switching node of inductor.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage (V+ – V-)		28	V
EN, LX Voltage		V_{IN}+0.3	V
FB, BS Voltage		6	V
Power Dissipation, P_D @ T_A = 25°C, TSOT23-6		1	W
Package Thermal Resistance	Θ_{JA}	100	°C/W
	Θ_{JC}	11.2	
Storage Temperature Range		-65 to 150	°C
Junction Temperature Range		150	°C
Lead Temperature Range		260	°C
HBM ESD, JESD22-A114	All Pins	±2	kV

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter	Rating	Unit
Supply Voltage	4.5 to 24	V
Junction Temperature Range	-40 to 125	°C
Ambient Temperature Range	-40 to 85	°C

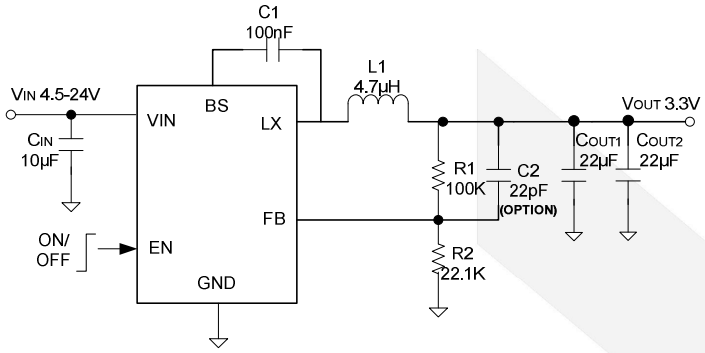
Electrical Characteristics

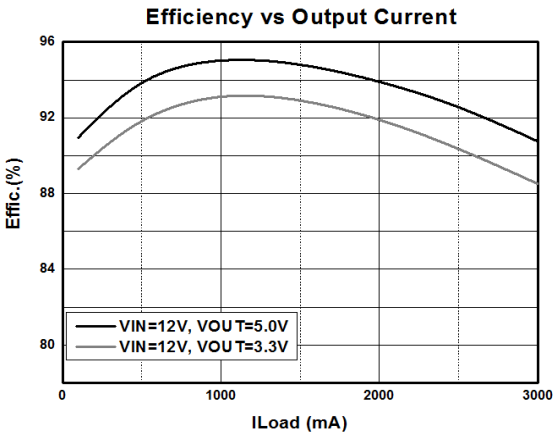
V_{IN} = 12V, V_{OUT} = 1.2V, L = 2.2μH, C_{OUT} = 47μF, T_A = 25°C, I_{OUT}=1A unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		4.5		24	V
I_Q	Quiescent Current	I_{OUT}=0, V_{FB}=V_{REF} · 105%		140		μA
I_{SHDN}	Shutdown Current	EN=0		5	10	μA
V_{REF}	Feedback Reference Voltage		0.591	0.6	0.609	V
I_{FB}	FB Input Current	V_{FB}=3.3V	-50		50	nA
$R_{DS(ON)}$	Top FET R_{ON}			80		mΩ
$R_{DS(ON)}$	Bottom FET R_{ON}			40		mΩ
I_{LIM}	Low side power FET current limit		3.0	4.0		A
V_{ENH}	EN Rising Threshold		1.5			V
V_{ENL}	EN Falling Threshold				0.4	V
V_{UVLO}	V_{IN} Under-Voltage Unlock Threshold, Rising				4.45	V
f_{SW}	Switching Frequency			500		kHz
	Min ON Time			40		ns
	Min OFF Time			180		ns
T_{SS}	Soft Start Time			1		ms
T_{SD}	Thermal Shutdown Temperature			148		°C
T_{HYS}	Thermal Shutdown Hysteresis			20		°C

Specifications subject to change without notice.

Typical Application

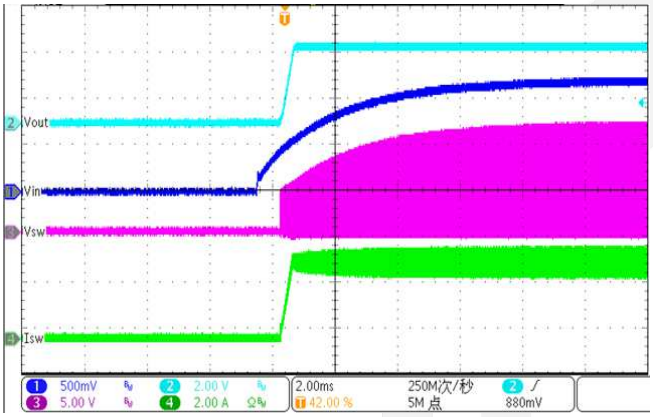




Typical Performance Characteristics

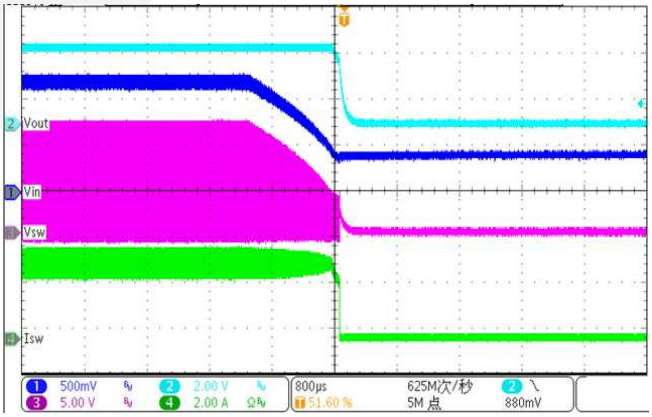
Start up from VIN

(V_{IN}=12V,V_{OUT}=3.3V,Load=1Ω)



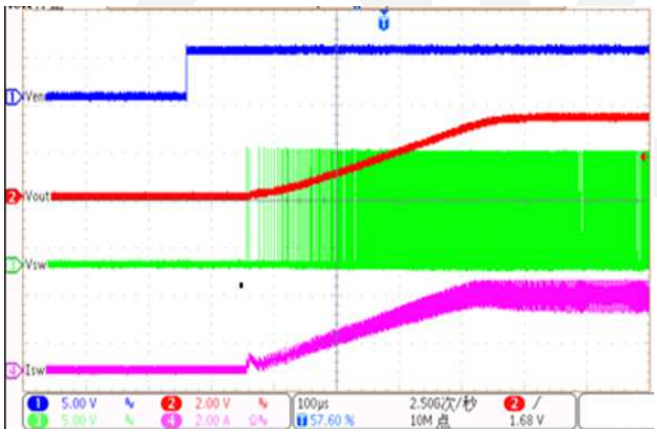
Shut down from VIN

(V_{IN}=12V,V_{OUT}=3.3V,Load=1Ω)



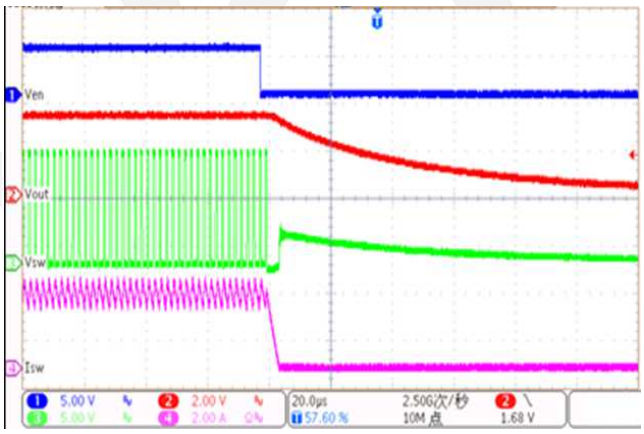
Start up from Enable

(V_{IN}=12V,V_{OUT}=3.3V,Load=1Ω)



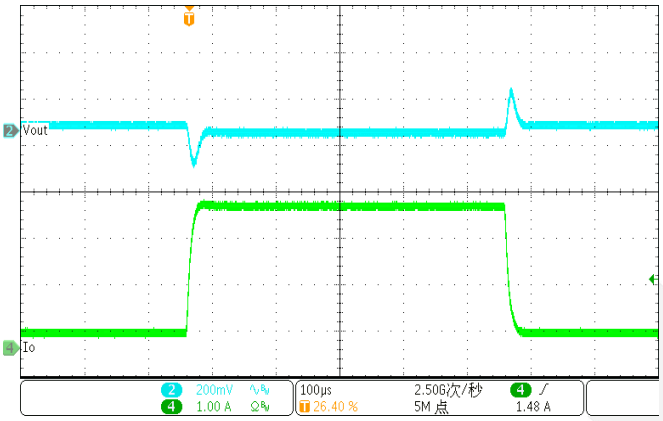
Shut down from Enable

(V_{IN}=12V,V_{OUT}=3.3V,Load=1Ω)



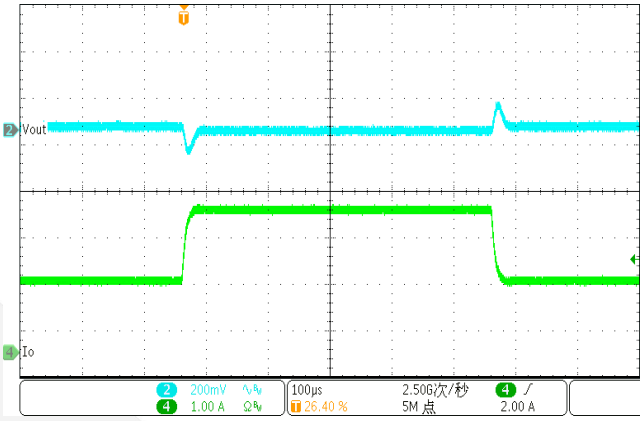
Load transient

(V_{IN}=12V,V_{OUT}=3.3V,Load=0.3-3A)



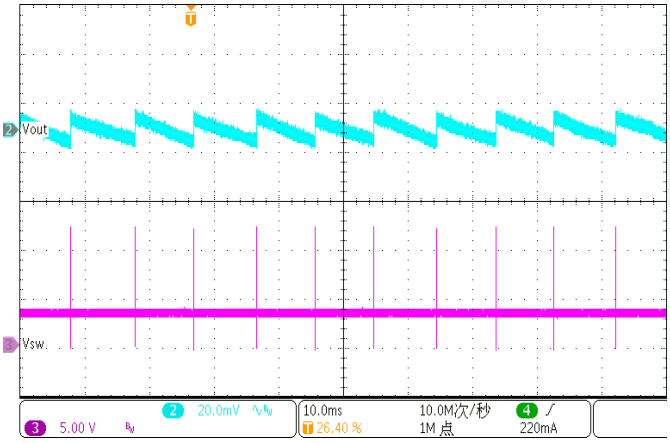
Load transient

(V_{IN}=12V,V_{OUT}=3.3V,Load=1.5-3A)



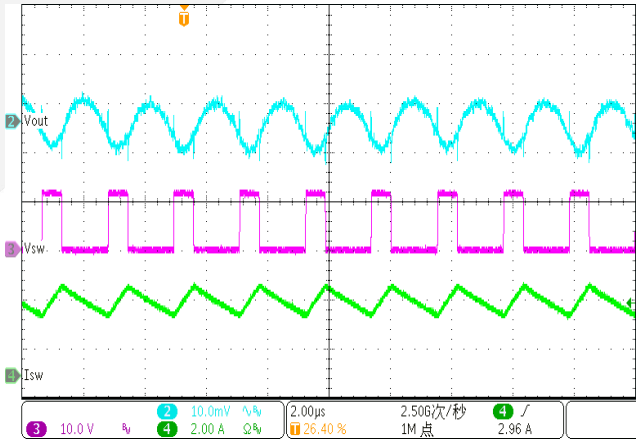
Ripple

(V_{IN}=12V,V_{OUT}=3.3V,Load=0A)



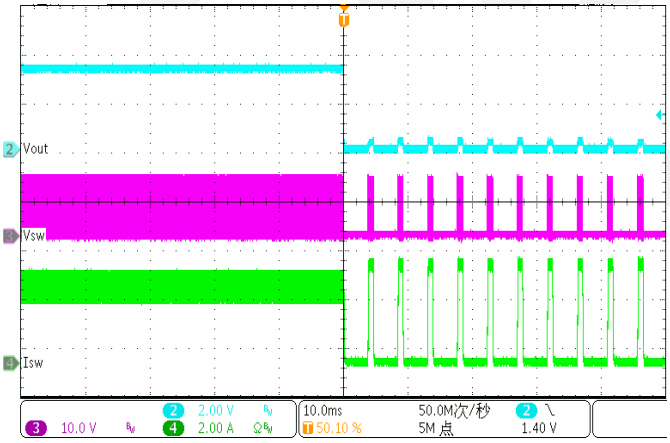
Ripple

(V_{IN}=12V,V_{OUT}=3.3V,Load=3A)



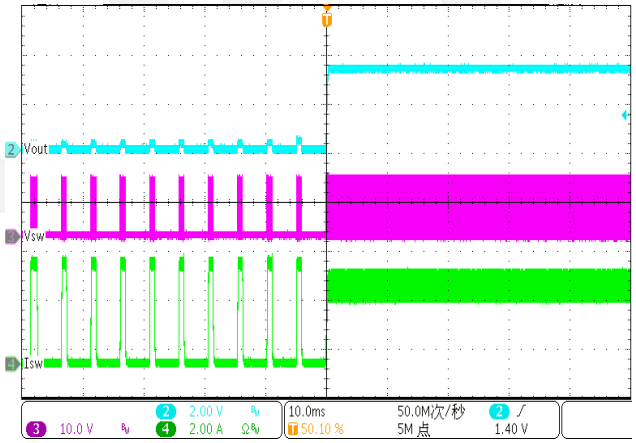
Short Circuit Protection

(V_{IN}=12V,V_{OUT}=3.3V,Load=3A)



Short Circuit Recovery

(V_{IN}=12V,V_{OUT}=3.3V,Load=3A)



Application Information

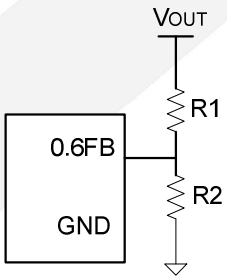
DIO6913 is a synchronous buck regulator IC that integrates the COT control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary COT control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

Because of the high integration in the DIO6913 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is highly recommended for both resistors. If Vout is 3.3V, R1=100k is chosen, then R2 can be calculated to be 22.1k.

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$



Input capacitor C_{IN}

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)}$$

This formula has a maximum at $V_{IN}=2V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$. This simple worst-case condition is commonly used for DC/DC design.

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22μF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L=\frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{F_{SW}\times I_{OUT,MAX}\times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current. The DIO6913 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN}>I_{OUT,MAX}+\frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2\cdot F_{SW}\cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

DIO6913 Recommended Table:

V_{OUT}(V)	R2(kΩ)	C2(pF)	L1/ Partnumber
1	150	Null	2.2μH/ SWPA6045S2R2NT (VLP6045-2R2M)
1.2	100	Null	2.2μH/ SWPA6045S2R2NT (VLP6045-2R2M)
1.8	49.9	Null	3.3μH/ SWPA8040S3R3NT (VLP6045-3R3M)
2.5	31.6	Null	3.3μH/ SWPA8040S3R3NT (VLP6045-3R3M)
3.3	22.1	22 (option)	4.7μH/ SWPA8040S4R7NT (CDRH8D43-4R7)
5	13.7	22 (option)	6.8μH/ SWPA8040S6R8MT (CDRH8D43-6R8)

Layout Design:

The layout design of DIO6913 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

CONTACT US

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