DIO69209
High-Efficiency 2A, 24V Input Synchronous Step Down Converter

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom) 120mΩ/75mΩ, 2.0A
- 4.5-24V input voltage range
- High-Efficiency Synchronous-Mode
- Internal soft start limits the inrush current
- Over Current protection
- Output short circuit protection with hiccup mode
- Thermal shutdown
- Green package:
  TSOT23 -6 is pin compatible

Applications

- Portable Navigation Device
- Set Top Box
- Portable TV
- LCD TV

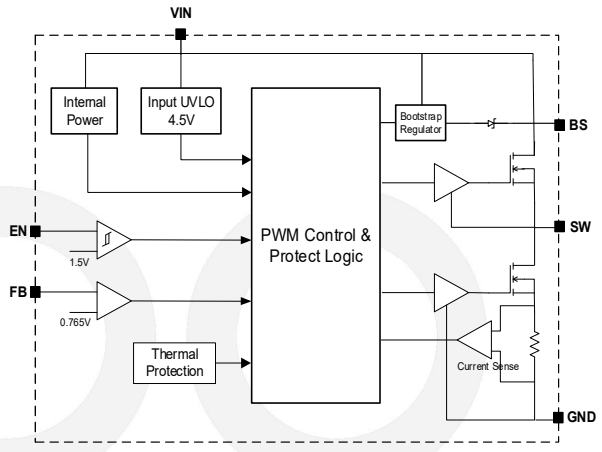
Descriptions

The DIO69209 is high-efficiency, high frequency synchronous step-down DC-DC regulator ICs capable of delivering up to 2A output currents. The DIO69209 family operate over a wide input voltage range from 4.5V to 24V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

DIO69209 adopts the pure COT architecture to achieve fast transient responses for high step down applications. In addition, it operates at pseudo-constant frequency of 500kHz under heavy load conditions to minimize the size of inductor and capacitor. The DIO69209 is stable with extremely low ESR, high capacitance.

DIO69209 always operate in continuous conduction mode, which reduces the output ripple voltage in light load compared to discontinuous conduction mode.

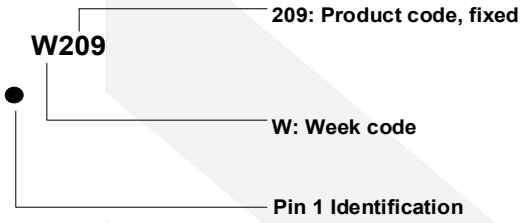
Function Block



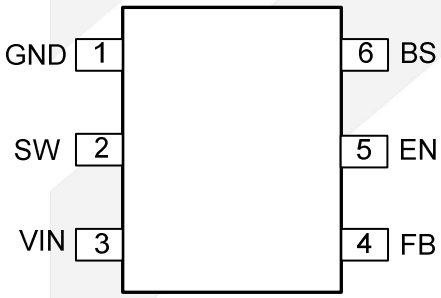
Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO69209TST6	W209	Green	-40 to 85°C	TSOT23-6	Tape & Reel, 3000

Marking Definition



Pin Assignments



TSOT23-6

Figure 1 Pin Assignment (Top View)

Pin Definitions

Pin Name	Description
GND	Power Ground
SW	Inductor pin. Connect this pin to the switching node of inductor.
VIN	Power Input
FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.765*(1+R1/R2).
EN	Enable control. Pull high to turn on. Do not float.
BS	Bootstrap. Connect a capacitor and a resistor between SW and BS pins to form a floating supply across the high-side switch driver. Recommend to use 0.1μF BS capacitor.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage (V+ – V-)		28	V
EN, SW Voltage		V_{IN}+0.3	V
FB Voltage		6	V
BS Voltage		SW+6	V
Package Thermal Resistance	Θ_{JA}	89	°C/W
	Θ_{JC}	44.5	
Storage Temperature Range		-65 to 150	°C
Junction Temperature Range		150	°C
Lead Temperature Range		260	°C

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter	Rating	Unit
Supply Voltage	4.5 to 24	V
Junction Temperature Range	-40 to 125	°C
Ambient Temperature Range	-40 to 85	°C

Electrical Characteristics

V_{IN} = 12V, V_{OUT} = 1.2V, L =2.2μH, C_{OUT} = 47μF, Tj = -40°C to 125°C, I_{OUT}=1A unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		4.5		24	V
I_Q	Quiescent Current	I_{OUT}=0, V_{FB}=V_{REF} · 105%		700	1000	μA
I_{SHDN}	Shutdown Current	EN=0		5	10	μA
V_{REF}	Feedback Reference Voltage	Tj = -40°C to 125°C	0.745	0.765	0.780	V
		Tj = 0°C to 125°C	0.750	0.765	0.780	
I_{FB}	FB Input Current	V_{FB}=V_{IN}	-50		50	nA
$R_{DS(ON)}$	Top FET R_{ON}	T_A = 25°C		120		mΩ
$R_{DS(ON)}$	Bottom FET R_{ON}	T_A = 25°C		75		mΩ
I_{LIM} (1)	Bottom FET Valley Current Limit		2.3	2.9	3.5	A
V_{ENH}	EN Rising Threshold		1.5			V
V_{ENL}	EN Falling Threshold				0.4	V
V_{UVLO}	Input UVLO Threshold		3.65	4.05	4.45	V
	Hysteresis V_{IN} voltage		0.3	0.4	0.5	V
f_{SW}	Switching Frequency		600	700	800	kHz
T_{ON}	ON Time	V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT}=1A		140		ns
	Min ON Time			50		ns
	Min OFF Time			90	140	ns
	Maximum Duty Cycle			90%		
T_{SS}	Soft Start Time		0.4	0.6	0.8	ms
T_{SD}	Thermal Shutdown Temperature			150		°C
T_{HYS}	Thermal Shutdown Hysteresis			15		°C

(1) Not production tested.

Specifications subject to change without notice.

Typical Application

DIO69209 4.5V to 24V Input, 1.05V Output Converter

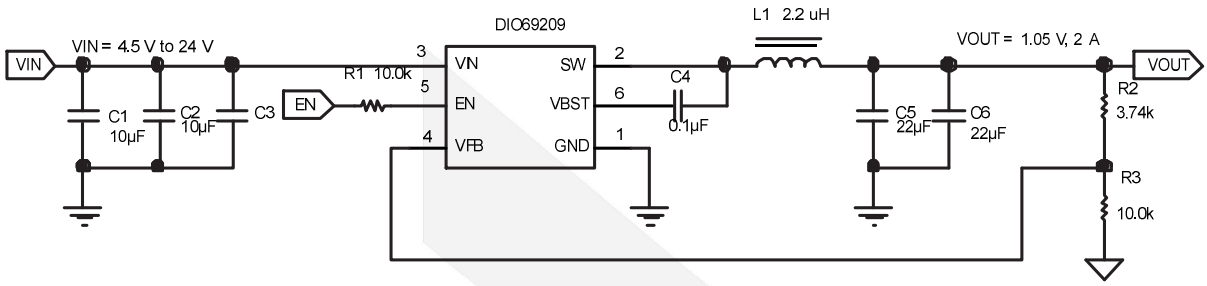
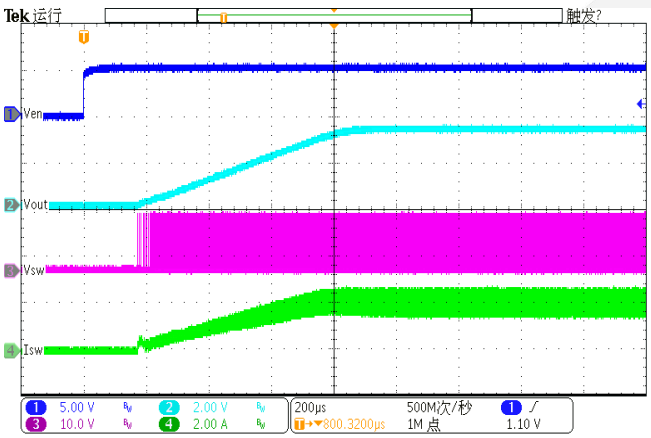


Figure 2. DIO69209 1.05V/2A Reference Design

Typical Performance Characteristics

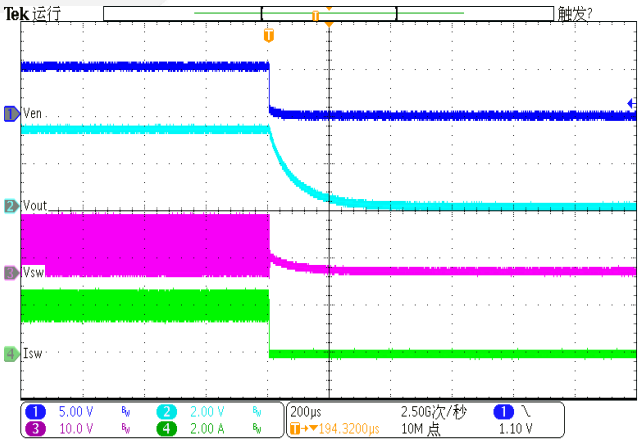
Start up from Enable

(V_{IN}=12V,V_{OUT}=3.3V,Load=1.5Ω)



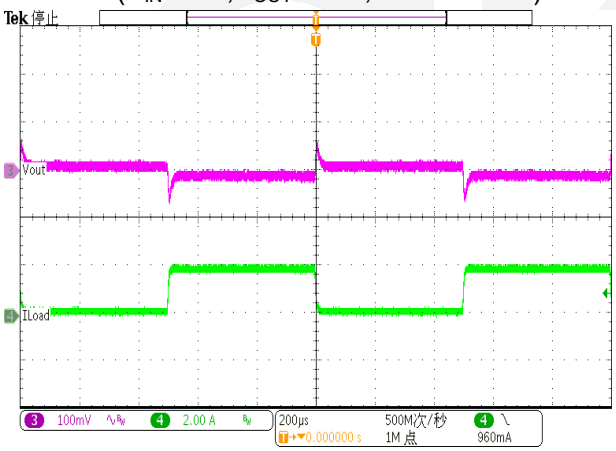
Shut down from Enable

(V_{IN}=12V,V_{OUT}=3.3V,Load=1.5Ω)



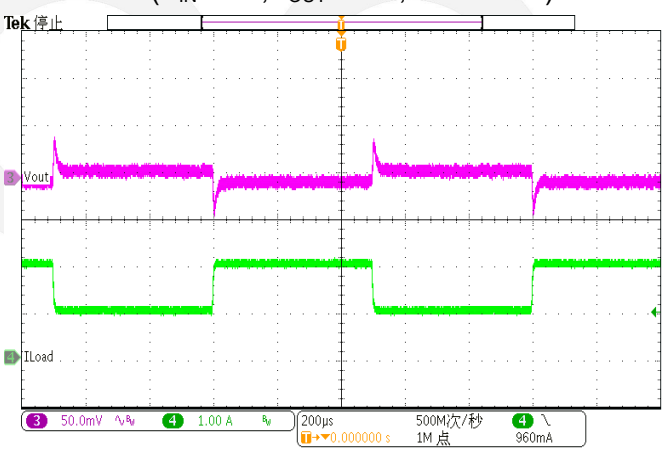
Load Transient

(V_{IN}=12V,V_{OUT}=3.3V,Load=0.2-2A)



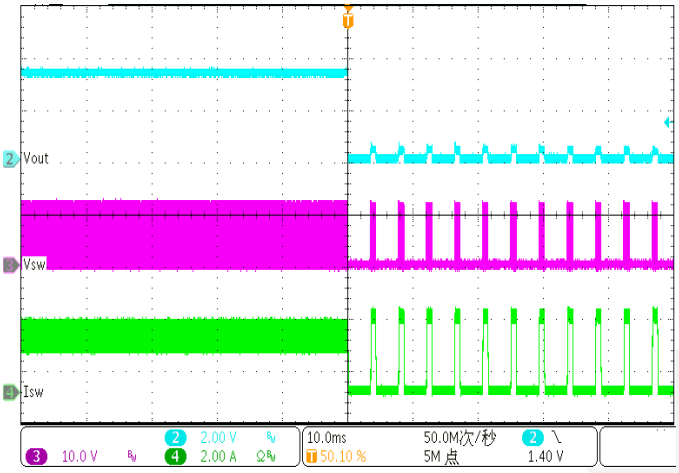
Load Transient

(V_{IN}=12V,V_{OUT}=3.3V,Load=1-2A)



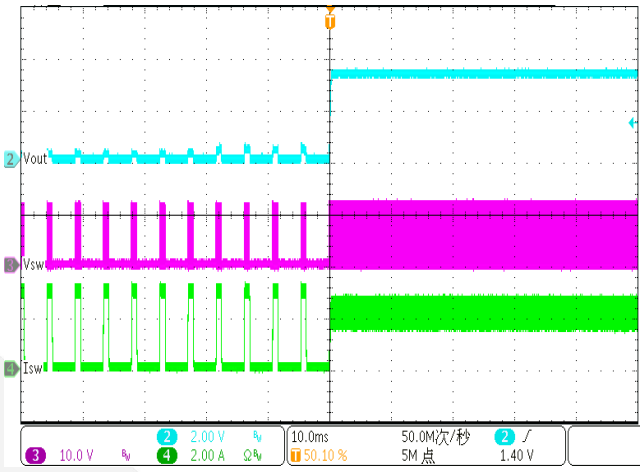
Short Circuit Protection

(V_{IN}=12V,V_{OUT}=3.3V,Load=2A)



Short Circuit Recovery

(V_{IN}=12V,V_{OUT}=3.3V,Load=2A)



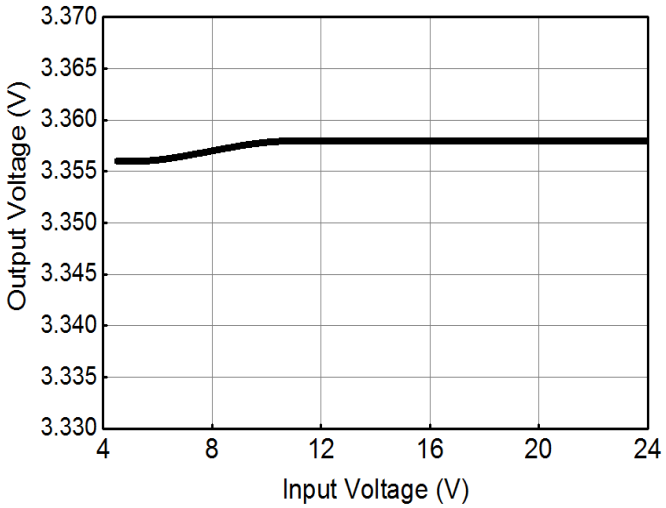
Line Regulation

(Vin=12V, Vout=3.3V, Iload=10mA)

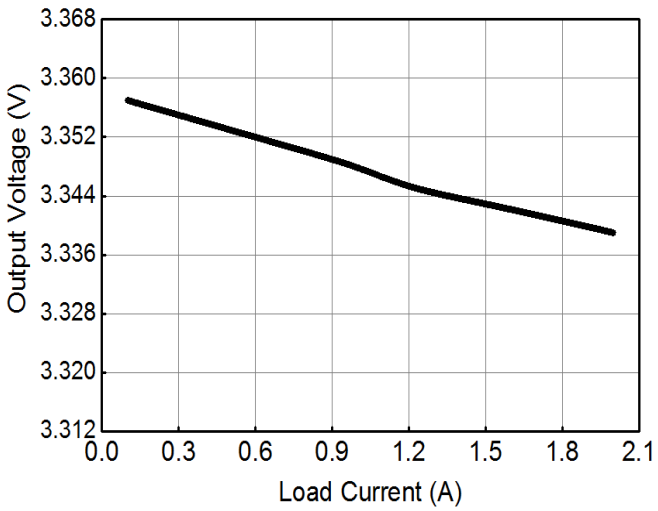
Load Regulation

(Vin=12V, Vout=3.3V)

Output Voltage vs. Input Voltage

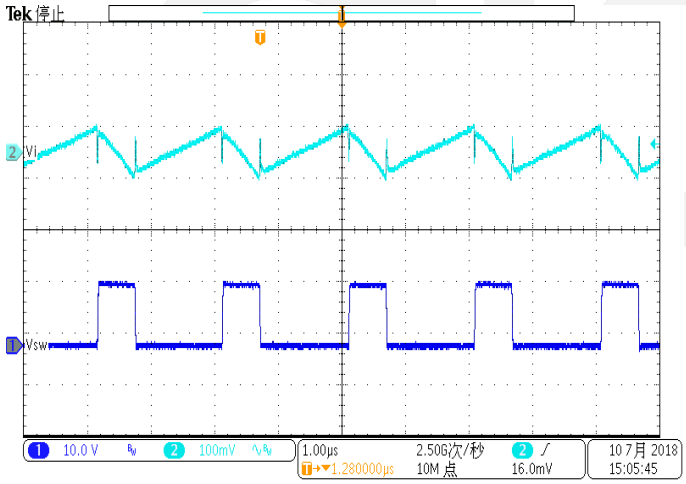


Output Voltage vs. Load Current



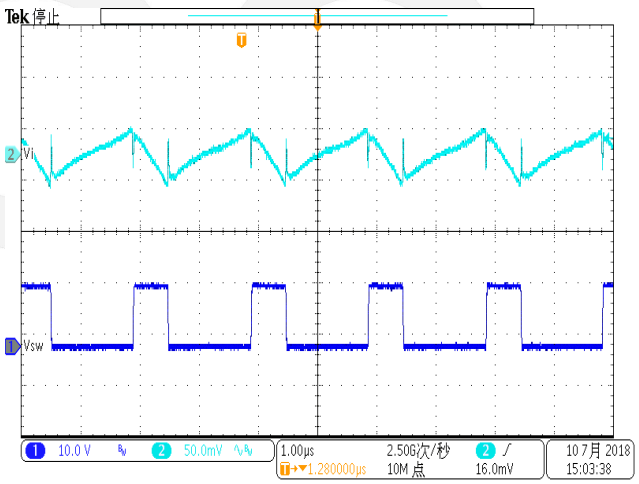
VIN Ripple

(Vin=12V, Load=2A, Cin=22uF)

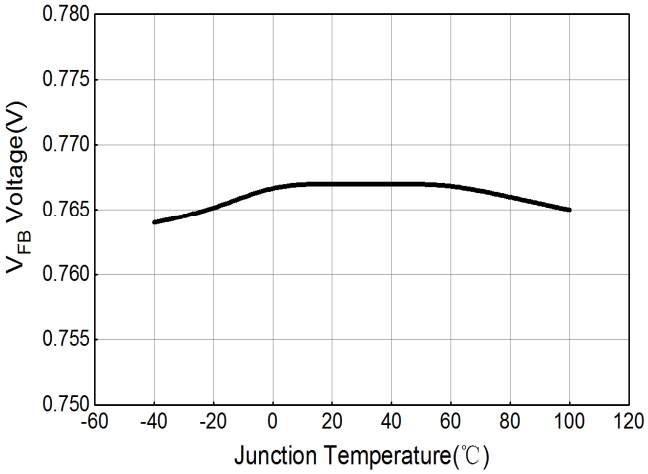


VIN Ripple

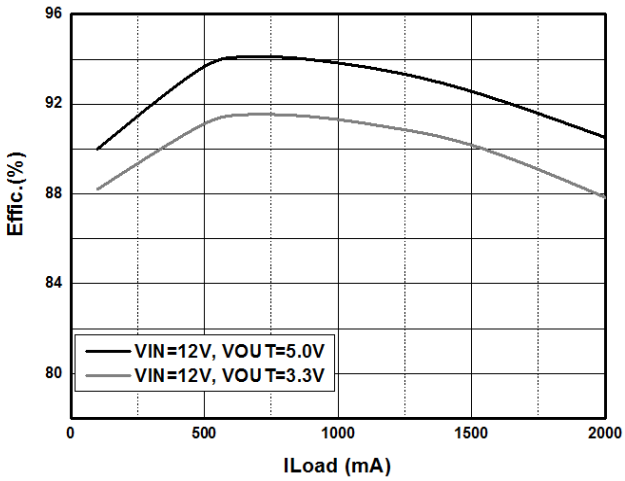
(Vin=12V, Load=2A, Cin=44uF)



V_{FB} vs. Temperature



Efficiency vs Output Current



Operation

DIO69209 is a synchronous buck regulator IC that integrates the pure COT control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary pure COT control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

DIO69209 provides protection functions such as cycle by cycle current limiting and thermal shutdown protection. DIO69209 will sense the output voltage conditions for the fault protection.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 V to 24 V
Output voltage	1.05 V
Output current	2 A
Output voltage ripple	20 mVpp

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R2 (kΩ)	R3 (kΩ)	L1 (μH)			C5 + C6 (μF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	44 - 66
1.05	3.74	10.0	1.5	2.2	4.7	44 - 66
1.2	5.76	10.0	1.5	2.2	4.7	44 - 66
1.5	9.53	10.0	1.5	2.2	4.7	44 - 66
1.8	13.7	10.0	1.5	2.2	4.7	44 - 66
2.5	22.6	10.0	2.2	3.3	4.7	44 - 66
3.3	33.2	10.0	2.2	3.3	4.7	44 - 66
5	54.9	10.0	3.3	4.7	4.7	44 - 66

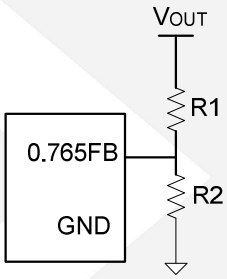
Applications Information

Because of the high integration in the DIO69209 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is highly recommended for both resistors. If V_{OUT} is 3.3V, R1=40.2k is chosen, then R2 can be calculated to be 12k.

$$R2 = \frac{0.765V}{V_{OUT} - 0.765V} R1$$



Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value.

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL threshold is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 14μs) and re-start after the hiccup time (typically 8ms).

When the over current condition is removed, the output voltage returns to the regulated value.

UVLO Protection

Under voltage lock out protection (UVLO) monitors the device input voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This is a non-latch protection.

Input capacitor C_{IN}

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS}=I_{OUT}\cdot\sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22μF capacitance.

Output inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L=\frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{F_{SW}\times I_{OUT,MAX}\times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The DIO69209 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

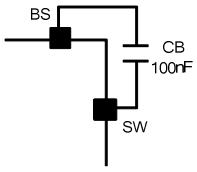
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN}>I_{OUT,MAX}+\frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2\cdot F_{SW}\cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

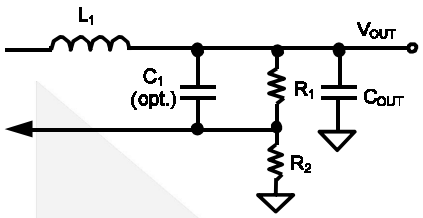
External Boostrap Cap

This capacitor provides the gate driver voltage for internal high side MOSFET. A 100nF low ESR ceramic capacitor connected between BS pin and SW pin is recommended.



Load Transient Considerations

The DIO69209 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient.



Layout Design

The layout design of DIO69209 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with SW pin must be minimized to avoid the potential noise problem.

4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

CONTACT US

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