

# DIO7330B

## 5.5V rated 2.4A capable slew rate controlled load switch

### Features

- 1.8V to 5.5V operation voltage range
- Low quiescent current < 1μA when disabled
- Reverse current blocking when switch is off
- Built-in 100Ω(typ) output discharge resistor
- 40mΩ N-MOSFET
- DC Current Up to 2.4A
- Peak Current Up to 5A
- Built-in Soft-Start 3ms
- Active High with Integrated Bridge
- Pb-Free Device DFN-4 1.2x1.6mm

### Applications

- Cell Phone and Digital Camera
- PDA and Notebook
- LCD Monitor
- TV and Set-Top Box

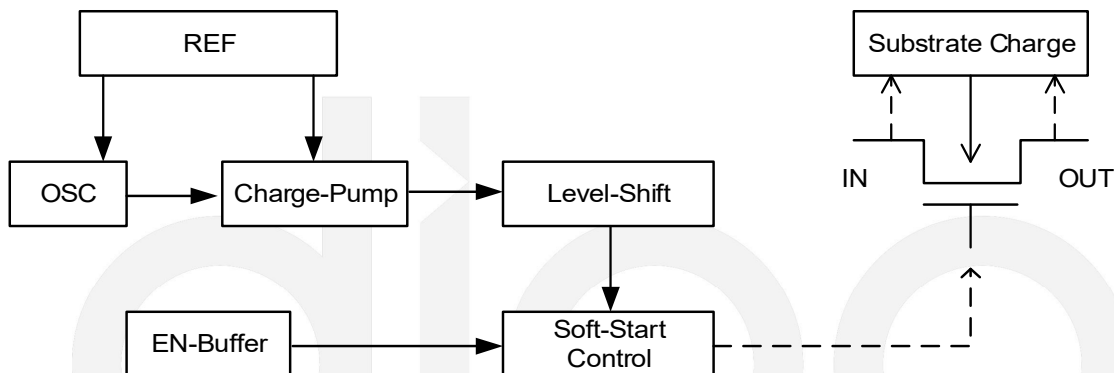
### Descriptions

The DIO7330B is a Low On-Resistance N-channel MOSFET controlled by a soft-start sequence of 3ms for mobile applications.

The low  $R_{DS(on)}$  allows system supplying or battery charging up to DC 2.4A. The device is enable automatically if a power supply is connected on  $V_{IN}$  pin (active High) and maintained off if no power input(internal pull down).

Due to the current consumption optimization, the leakage current is drastically decreased from the battery connected to the device, which allows extending the battery life.

### Block Diagram



### Ordering Information

Order Part Number	Top Marking		$T_A$	Package	
DIO7330BDN4	YW3B	Green	-40 to 85°C	TDFN-4	Tape & Reel, 3000

## Pin Assignments

DFN-4 (TOP VIEW)

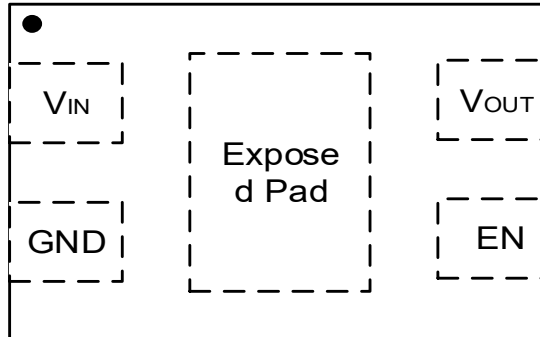


Figure 1 Pin Assignment

## Pin Description

Pin	Name	Type	Description
1	V <sub>IN</sub>	Power	Switch Input voltage; connect a 1μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
2	GND	Power	GND.
3	EN	Input	Enable input, logic high active.
4	V <sub>OUT</sub>	Output	Switch Output; connect a 1μF capacitor from V <sub>OUT</sub> to GND as close as possible to the IC.
	Exposed Pad	Power	Exposed pad can be connected to GND plane for dissipation purpose or any other thermal plane.



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## Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
V <sub>IN</sub>		-0.3 to 6	V
V <sub>OUT, EN</sub>		-0.3 to 6	V
Storage Temperature		-65 to 150	°C
Maximum Junction Range		-40 to 145	°C
Thermal Resistance, $\theta_{JA}$		170	°C/W
Power Dissipation, (T <sub>A</sub> =25°C)		580	mW
Latch Up Protection		200	mA
ESD	HBM, JEDEC: JESD22-A114	6	kV
	CDM, JEDEC : JESD22-C101	2	

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>IN</sub>	Operational Power Supply		1.8		5.5	V
V <sub>EN</sub>	Enable Voltage		0		5.5	V
C <sub>IN</sub>	Decoupling input capacitor		1			μF
C <sub>OUT</sub>	Decoupling output capacitor	USB port per Hub	1			μF
I <sub>OUT</sub>	Maximum DC Current	T <sub>A</sub> =25°C			3	A
I <sub>PEAK</sub>	Maximum Peak Current	1ms pulse width at 217Hz ,T <sub>A</sub> =25°C			5	A
T <sub>A</sub>	Ambient Temperature Range		-40	25	85	°C
T <sub>J</sub>	Junction Temperature Range		-40	25	125	°C



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## Electrical Characteristics

$T_A=25^{\circ}\text{C}$   $V_{IN}=5\text{V}$ , unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>POWER SWITCH</b>						
$R_{DS(ON)}$	Static drain-source on-state resistance	$V_{IN}=1.8\sim 5.5\text{V}$ , $T_A = 25^{\circ}\text{C}$		40		m $\Omega$
		$I_{OUT}=200\text{mA}$ , $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$			70	m $\Omega$
$t_R$	Switch turn-on edge rising time	$V_{IN}=4.5\text{V}$ $C_{LOAD}=100\mu\text{F}$ , $R_{LOAD}=150\Omega$	2	2.5	5	ms
$t_F$	Switch turn-off edge falling time	$V_{IN}=4.5\text{V}$ $C_{LOAD}=100\mu\text{F}$ , $R_{LOAD}=150\Omega$		3		ms
$t_{DON}$	Switch turn-on delay	$V_{IN}=4.5\text{V}$ ; $C_{LOAD}=100\mu\text{F}$		1.5		ms
$t_{DOFF}$	switch turn-off delay	$V_{IN}=4.5\text{V}$ ; $C_{LOAD}=100\mu\text{F}$		10		$\mu\text{s}$
<b>ENABLE INPUT EN</b>						
$V_{IH}$	High-level input voltage		1.45			V
$V_{IL}$	Low-level input voltage				0.85	V
$R_{PD}$	Pull-down resistance at EN pin	$T_A = -45^{\circ}\text{C}$ to $85^{\circ}\text{C}$		1		M $\Omega$
<b>REVERSE-LEAKAGE PROTECTION</b>						
$I_{REV}$	Reverse-current protection	$V_{IN}=0\text{V}$ , $V_{OUT}=4.2\text{V}$ , $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ , $EN="0"$		1	2	$\mu\text{A}$
<b>QUIESCENT CURRENT</b>						
$I_Q$	Current consumption	$V_{IN}=5\text{V}$ , $V_{OUT}$ floating, $EN=5\text{V}$		100	180	$\mu\text{A}$
$I_{SDN}$	shutdown current	$V_{IN}=5\text{V}$ , $En="0"$ , $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$			1	$\mu\text{A}$
$R_{DR}$	Output Discharge resistor	$V_{IN}=5\text{V}$ , $En="0"$		100		$\Omega$

**Note:** This parameter is guaranteed by design and characterization.



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### Application Information

#### Enable

Enable pin voltage in the active high means on. This part is automatically turned on when the input voltage enables the device. In the other side, this part is turned off when the input voltage is not available, which limits current consumption from battery to  $V_{OUT}$  pin.

#### Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, an input capacitor is placed to the  $V_{IN}$  and GND as close as possible. The value of the input capacitor is recommended  $1\mu\text{F}$  at least. Higher values capacitor can help to further reduce the voltage drop.

#### Output Capacitor

While the device works, a capacitor from  $100\text{nF}$  to  $1\mu\text{F}$  across  $V_{OUT}$  and GND is recommended to accommodate load transient condition. It also helps to prevent parasitic inductance forces  $V_{OUT}$  below GND when switching off. Output capacitor has the minimal effect on device's turn on slew rate time.

#### Blocking Control

The blocking control circuitry switches the bulk of the power NMOS. When the part is off (No  $V_{IN}$  or EN tied to GND externally), the body diode limits the leakage current  $I_{REV}$  from OUT to IN. In this condition, the anode of the body diode is connected to IN pin and the cathode is connected to OUT pin. During the operation, the anode of the body diode is connected to OUT pin and the cathode is connected to IN pin to prevent the discharge of the power supply.





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## CONTACT US

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